



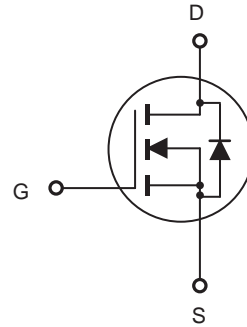
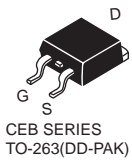
CEP07N65A/CEB07N65A CEF07N65A

N-Channel Enhancement Mode Field Effect Transistor

FEATURES

Type	V _{DSS}	R _{DS(ON)}	I _D	@V _{GS}
CEP07N65A	650V	1.45Ω	7A	10V
CEB07N65A	650V	1.45Ω	7A	10V
CEF07N65A	650V	1.45Ω	7A ^d	10V

- Super high dense cell design for extremely low R_{DS(ON)}.
- High power and current handling capability.
- Lead-free plating ; RoHS compliant.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V _{DS}	650		V
Gate-Source Voltage	V _{GS}	±30		V
Drain Current-Continuous @ T _C = 25 C @ T _C = 100°C	I _D	7	7	A
		5	5 ^d	A
Drain Current-Pulsed ^a	I _{DM} ^e	28	28 ^d	A
Maximum Power Dissipation @ T _C = 25°C - Derate above 25°C	P _D	150	48	W
		1	0.5	W/°C
Single Pulsed Avalanche Energy ^h	E _{AS}	150		mJ
Single Pulsed Avalanche Current ^h	I _{AS}	5		A
Operating and Store Temperature Range	T _J , T _{stg}	-55 to 175		°C

Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	R _{θJC}	1	3.1	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	65	°C/W



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Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	650			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650V, V_{GS} = 0V$			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
On Characteristics^b						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 3A$		1.15	1.45	Ω
Gate input resistance	R_g	f=1MHz, open Drain		1.5		Ω
Dynamic Characteristics^c						
Input Capacitance	C_{iss}	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0 \text{ MHz}$		1410		pF
Output Capacitance	C_{oss}			115		pF
Reverse Transfer Capacitance	C_{rss}			15		pF
Switching Characteristics^c						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300V, I_D = 6A,$ $V_{GS} = 10V, R_{GEN} = 25\Omega$		26	52	ns
Turn-On Rise Time	t_r			58	116	ns
Turn-Off Delay Time	$t_{d(off)}$			85	170	ns
Turn-Off Fall Time	t_f			63	126	ns
Total Gate Charge	Q_g		$V_{DS} = 480V, I_D = 6A,$ $V_{GS} = 10V$		28	36
Gate-Source Charge	Q_{gs}			6		nC
Gate-Drain Charge	Q_{gd}			9		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current	I_S^f				7	A
Drain-Source Diode Forward Voltage ^b	V_{SD}	$V_{GS} = 0V, I_S = 3A^g$			1.5	V
Notes : □ a.Repetitive Rating : Pulse width limited by maximum junction temperature . b.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. □ c.Guaranteed by design, not subject to production testing. □ d.Limited only by maximum temperature allowed . e.Pulse width limited by safe operating area . f.Full package $I_{S(max)} = 1A$. g.Full package V_{SD} test condition $I_S = 1A$. □ h.L = 12mH, $I_{AS} = 5A, V_{DD} = 50V, R_G = 25\Omega$, Starting $T_J = 25 \text{ C}$.						



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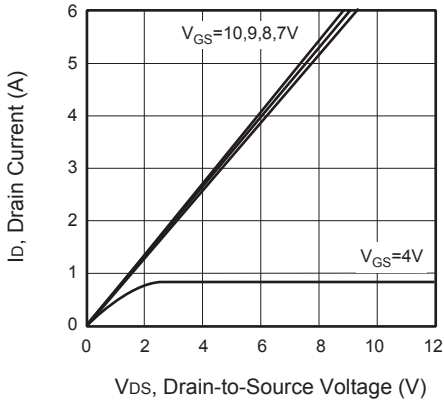


Figure 1. Output Characteristics

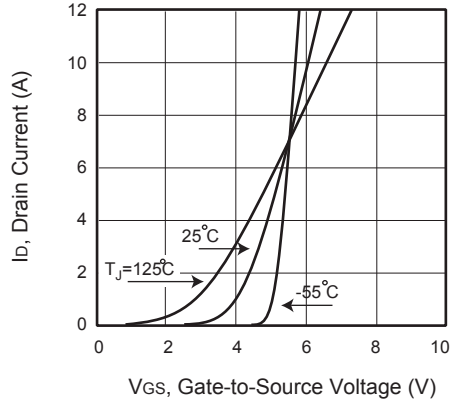


Figure 2. Transfer Characteristics

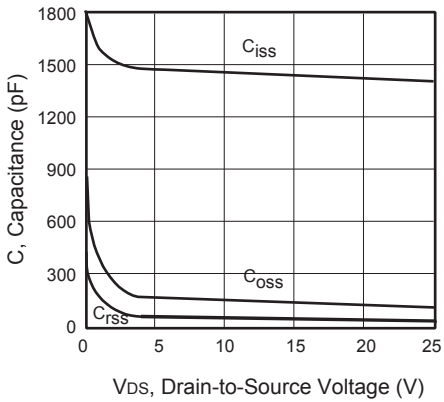


Figure 3. Capacitance

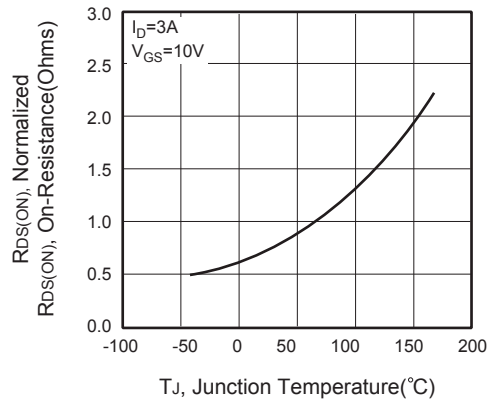


Figure 4. On-Resistance Variation with Temperature



Figure 5. Gate Threshold Variation with Temperature

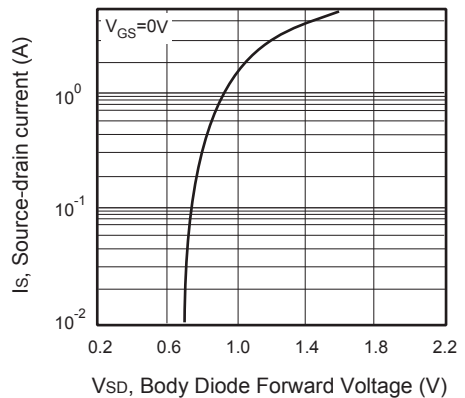


Figure 6. Body Diode Forward Voltage Variation with Source Current



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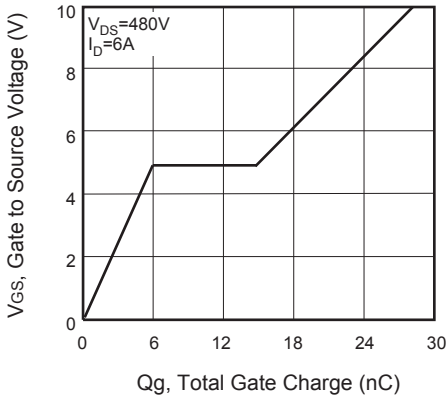


Figure 7. Gate Charge

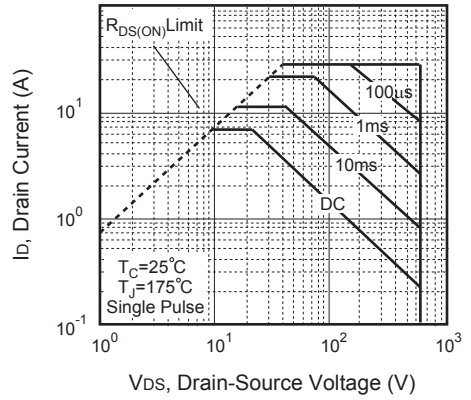


Figure 8. Maximum Safe Operating Area



Figure 9. Switching Test Circuit



Figure 10. Switching Waveforms

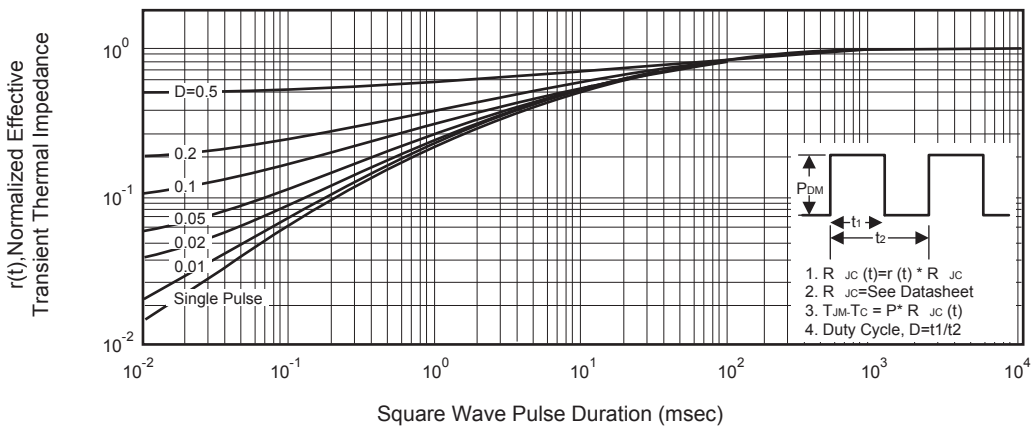


Figure 11. Normalized Thermal Transient Impedance Curve